REMARKS

Claims 1-3, 6-13, and 15-22 are now present in this application.

Claims 1, 11 and 16 have been amended, and claims 21 and 22 have been presented. Reconsideration of the application, as amended, is respectfully requested.

Claims 1-3, 6-13, 15-18 and 20 stand rejected under 35 USC 103 as being unpatentable over Applicant's admitted prior art in view of KER et al., U.S. Patent 5,959,820. This rejection is respectfully traversed.

Claim 1 recites an electrostatic discharge protection device located between a pad and an internal circuit, and coupled between a first power wire and a second power wire, comprising: a switching circuit for outputting an enable signal when receiving a detecting result signal; a voltage detecting device comprising at least one serial diode connected between the first power wire and the switching circuit, and outputting the detecting result signal when a voltage level of the first power wire reaches a first predetermined voltage level; a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch includes a first controlling gate connected to the second power wire and is turned on when a voltage level of the pad reaches a second predetermined voltage level; a second switch coupled to the connection point between the pad and the internal circuit,

wherein the second switch includes a second controlling gate connected to the first power wire and is turned on when the voltage level of the pad reaches a third predetermined voltage level lower than the second predetermined voltage level; a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch includes a third controlling gate; and a driving circuit coupled to the switching circuit for outputting a ground level signal to the third controlling gate and causing the third switch to electrically break down concurrent with the first switch when the driving circuit receives the enable signal and the voltage level of the pad reaches the second predetermined voltage level.

Claim 11 recites an electrostatic discharge protection device located between a pad and an internal circuit, and coupled to a first power wire, a second power wire, and a third power wire, comprising: a switching circuit for outputting an enable signal when receiving a detecting result signal; a voltage detecting device comprising at least one serial diode connected between the third power wire and the switching circuit, and outputting the detecting result signal when a voltage level of the third power wire reaches a first predetermined voltage level; a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch includes a first controlling gate connected to the second power wire and is turned on when a voltage

level of the pad reaches a second predetermined voltage level; a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch includes a second controlling gate connected to the first power wire and is turned on when the voltage level of the pad reaches a third predetermined voltage level lower than the second predetermined voltage level; a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch includes a third controlling gate; and a driving circuit coupled to the switching circuit for outputting a ground level signal to the third controlling gate and causing the third switch to electrically break down concurrent with the first switch when the driving circuit receives the enable signal and the voltage level of the pad reaches the second predetermined voltage level.

The Applicant's admitted prior art discloses an electrostatic discharge protection device located between a pad and an internal circuit, and coupled to a first power wire, a second power wire, and a third power wire, comprising: a switching circuit; a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch includes a first controlling gate connected to the second power wire and is turned on when a voltage level of the pad reaches a second predetermined voltage level; a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch

includes a second controlling gate connected to the first power wire and is turned on when the voltage level of the pad reaches a third predetermined voltage level lower than the second predetermined voltage level; a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch includes a third controlling gate; and a driving circuit coupled to the switching circuit, the third power wire and the third controlling gate.

The Applicant's admitted prior art does not disclose a switching circuit for outputting an enable signal when receiving a detecting result signal. The Applicant's admitted prior art also does not a voltage detecting device comprising at least one serial diode connected between the first or the third power wire and the switching circuit, and outputting a detecting result signal when a voltage level of the first or the third power wire reaches a first predetermined voltage level.

In addition, the Applicant's admitted prior art does not disclose a driving circuit for outputting a ground level signal to the third controlling gate and causing the third switch to electrically break down concurrent with the first switch when the driving circuit receives the enable signal and the voltage level of the pad reaches the second predetermined voltage level.

The problems of the Applicant's admitted prior art are that NMOS transistors (M20A, M21A, M22A and M23A) do not break down at

the same time to release the ESD current when the driving circuit provides a high voltage level signal to the gates of NMOS transistors M22A and M23A. If only NMOS transistors M22A and M23A are turned on, the probability of breakdown of the NMOS transistors M20A and M21A is extremely low. Thus, massive ESD current flows to ground through NMOS transistors M22A and M23A, decreasing ESD current discharge ability (see page 4, lines 5-20, for example). In addition, the massive ESD current damages the gate oxide of NMOS transistors M22A and M23A.

Thus, a voltage detecting device comprising at least one serial diode connected between the first or the third power wire for outputting the detecting result signal when a voltage level of the first or the third power wire reaches a first predetermined voltage level, a switching circuit for outputting an enable signal when receiving the detecting result signal, and a driving circuit for outputting a ground level signal to the third controlling gate and causing the third switch to electrically break down concurrent with the first switch when the driving circuit receives the enable signal and the voltage level of the pad reaches the second predetermined voltage level, are provided by the present invention to solve the problems of the Applicant's admitted prior art. The problems of the Applicant's admitted prior art are solve because the gates of NMOS transistors (M50A, M51A, M52A and M53A) are all grounded (see Fig. 3, for example). Thus, NMOS transistors (M50A,

M51A, M52A and M53A) break down at the same time as the voltage level of the pad reaches the second predetermined voltage level.

KER et al. teaches a voltage based ESD detection circuit and provides multiple ways for implantation of such ESD detection circuits including a diode string. The ESD detection circuit of KER et al. detects the electrostatic discharge at the power supplies and triggers the control gates of the cascade LVSCR to dissipate the electrostatic discharge.

KER et al. does not disclose a voltage detecting device comprising at least one serial diode connected between a power wire and the switching circuit (202), wherein the switching circuit (202) outputs an enable signal when receiving a detecting result signal provided by the voltage detecting device. The switching circuit (202) of KER et al. is triggered to dissipate the electrostatic discharge, not output an enable signal to direct the driving circuit to output a ground level signal to the third controlling gate and cause the third switch to electrically break down concurrent with the first switch when the voltage level of the pad reaches the second predetermined voltage level.

Thus, one of ordinary skill in the art cannot add the ESD detection circuit of KER et al. between the power wire and the switching circuit of the Applicant's admitted prior art.

In addition, whereas the problems of the Applicant's admitted prior art are not disclosed in KER et al., one of ordinary skill in

the art cannot infer the present invention by combining the Applicant's admitted prior art and KER et al.

Neither the Applicant's admitted prior art nor KER et al., either alone or in combination, teaches or suggests the switching circuit for outputting an enable signal when receiving a detecting result signal, a voltage detecting device comprising at least one serial diode connected between the first or the third power wire and the switching circuit and outputting the detecting result signal when a voltage level of the first or the third power wire reaches a first predetermined voltage level, or a driving circuit for outputting a ground level signal to the third controlling gate and causing the third switch to electrically break down concurrent with the first switch when the driving circuit receives the enable signal and the voltage level of the pad reaches the second predetermined voltage level.

It is noted that the Examiner states that internal circuit 42 does require ESD protection because the high voltage level signal output from the driving circuit 48 opens (turns on) FETs M52A and M53A and connects an input of internal circuit 42 to the ground when switch circuit 46 does not receive input signals. The Applicants respectfully point out that this statement of the Examiner is incorrect. As mentioned, disadvantages of the Applicant's admitted prior art include ESD current concentrated on turning on FETs and decreasing ESD current discharge ability, and

the massive ESD damaging turned-on FETs. To solve this problem, FETs M50A, M51A, M52A and M53A are all turned off by the driving circuit according to the detecting result signal output from the voltage detecting device when a voltage level of the power wire reaches a predetermined voltage level, and the *electrical breakdown* of the FETs occurs at the same time, such that ESD current is dissipated by the FETs M50A, M51A, M52A and M53A, not only FETs M52A and M53A. Thus, the amplitude of ESD current distributed to each FETs is decreased.

In view of the foregoing amendments and remarks, it is respectfully submitted that the claims of the present invention are neither taught nor suggested by the prior art utilized by the Examiner. Reconsideration and withdrawal of the 35 USC 103 rejection are therefore respectfully requested.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

In the event the Examiner does not consider this application to be in condition for allowance, it is respectfully requested that this Amendment be entered for the purposes of Appeal. This Amendment should overcome the current grounds of rejection and therefore simplify the issues for Appeal. Nonetheless, it should be unnecessary to proceed to Appeal because the instant application should now be in condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Joe McKinney Muncy, #32,334

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

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